

# Independently-Controlled-Gate FinFET 6T SRAM Cell Design for Leakage Current Reduction and Enhanced Read Access Speed

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**Abstract**—In this paper, two novel 6T SRAM cells based on Independently-Controlled-Gate FinFETs are proposed. The new 6T cells are derived from 4T cells: by separating the read timing and read-line, the proposed new cells allow simultaneously read & write to different addresses. To overcome the traditional retention time problem in 4T cells, the proposed cells reduce leakage by changing the back-gate connection and increasing the capacitance at data storage points (Q, QB). Compared to previous 6T FinFET SRAMs, the proposed cells reduce the static leakage current, and enhance the write and read speed. In addition, this structure is scalable for multi-ports.

**Keywords**—Independently-Controlled-Gate, FinFET, SRAM, Leakage Current Reduction, Static Noise Margin, Read Speed.

## I. INTRODUCTION

With the sharp increase of portable electronic applications, power dissipation has become one of the most important design factors in the deep sub-micron VLSI design [1-3]. With short channel effects (SCEs) becoming intolerable with the transistor channel length scaling, multi-gate devices have been proposed to overcome SCEs and extend the technology roadmap. FinFET (Fin-type Field-effect Transistor) has emerged as the most feasible multi-gate device due to process compatibility with bulk CMOS technology [2]. Because of the drastic leakage reduction and performance improvement compared to planar CMOS, FinFET technology has been applied to both high performance and low power applications [1-3], especially for Static Random Access Memory (SRAM) design due to its low STANDBY-by power requirement [4]. Numerous techniques have been explored to improve the energy efficiency of FinFET SRAM considering the frequent access of SRAM bit-cells and the essential portion of the chip area [4]. Thus, it is important to explore the FinFET SRAM cell designs to further improve power efficiency [5].

Many techniques have been proposed to reduce leakage, improve stability and access speed in FinFET SRAM design. These techniques can be summarized into several categories: (1) at the device level, by introducing the advanced device technologies in FinFET device designs to improve SRAM density, stability [4, 6] and energy efficiency [5]; (2) At the circuit level, by adding additional transistors to cells to enhance stability [10] and noise margins [11], or (3) by using the back-gate feature. For example, independent gate techniques have been proposed on pass-transistors to enhance the stability [8] and to overcome process and environmental variations [9]. Also, the back-gate feature within FinFET SRAM cells has been explored in [12-16] to reduce the leakage and improve performance.

In this paper, we explore the circuit level optimization to FinFET SRAM cells to reduce the leakage, improve the noise margins, and enhance the read speed, without sacrificing the area. We propose two novel 6-Transistor (6T) FinFET SRAM cell designs based on the independent-controlled-gate technique [1-4] using 32nm FinFET Predictive Technology Model (PTM) [31]. Compared to the traditional 6T SRAM design, our proposed design exhibits over 80% leakage reduction, much better margins, and read speed improvement.

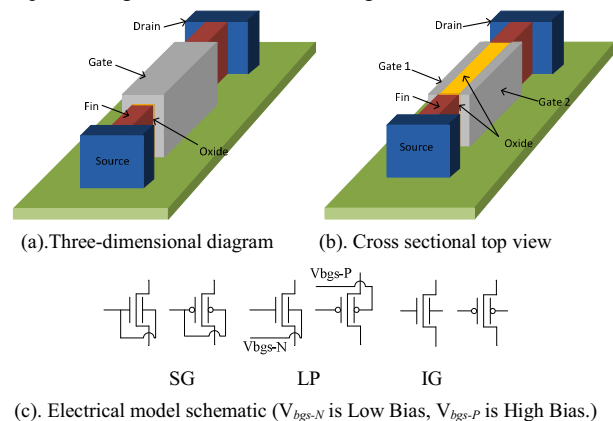
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The paper is organized as follows. In Section II, we introduce the physical FinFET devices with the back-gate voltage and dynamic threshold control feature. Section III summarizes the previous FinFET SRAM cell designs. Section IV describes the proposed SRAM cells and solutions for possible multi-port scalability. The simulation result, including the leakage power and retention time, Static Noise Margin (SNM) and read & write time are presented in Section V, showing the proposed layout designs as compared to the traditional 6T cells. Section VI verifies an 8K\*128 scale SRAM array with all necessary peripheral circuits, followed by the conclusions in Section VII.

## II. FINFET DEVICES

Fig. 1 (a) illustrates the three-dimensional schematic of a typical shorted-gate FinFET transistor. The thin vertical silicon fin is the conductive channel and the metal gate wraps the fin to control the channel effectively. Because of the multi-gate induced electrostatic improvement, FinFETs suppress the SCEs and offer higher on-state current, lower off-state current and faster switching speed.

FinFETs come in many flavors. In Shorted-Gate (SG) FinFETs, the two gates are connected together. This can serve as a direct replacement for conventional bulk-CMOS devices. In independent-gate (IG) FinFETs, the top part of the gate is etched out, giving way to two independent gates (Fig. 1 (b)). Because the two independent gates can be controlled separately, IG-mode FinFETs offer more design options [1]. In general, three modes of FinFET logic gates are logically obvious (Fig. 1 (c)) [1-3]: (1) Shorted-Gate mode (SG), in which FinFET gates are tied together; (2) Low-Power mode (LP), in which the back-gate bias is tied to a reverse-bias voltage to reduce sub-threshold leakage [1]; (3) Independent-Gate mode (IG), in which independent signals drive the two device gates.



(c). Electrical model schematic ( $V_{bgs-N}$  is Low Bias,  $V_{bgs-P}$  is High Bias.)

**Figure 1.** FinFET device schematic and model illustration.

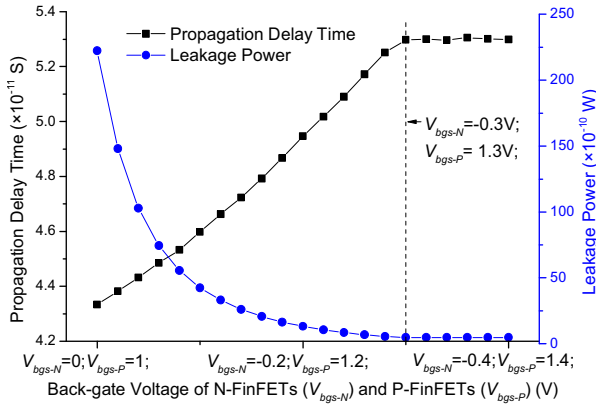
In Fig. 1 (b), considering the gate-gate coupling of the front and back gate, threshold voltage of the front-gate varies in response to the back-gate bias voltage. A generalized model for the relationship between FinFET front-gate threshold voltage and the applied back gate voltage is derived in [12]. Equation (1) demonstrates the

approximate relationship.

$$V_{thfg-N} \approx \begin{cases} V_{thfg-N}^0 - \delta * (|V_{gbs-N}| - V_{thbg-N}) \cdots \text{when } |V_{gbs-N}| < V_{thfg-N}^0 \\ V_{thfg-N}^0 \cdots \text{otherwise} \end{cases} \quad (1)$$

Where  $V_{bgs-N}$  is back gate voltage, and  $V_{bgs-N} \leq 0$ ,  $V_{thfg-N}$  and  $V_{thbg-N}$  STANDBY for the threshold of the N-FinFET front gate and back gate respectively.  $s$  denotes the source terminal of FinFET,  $\delta$  is a positive value determined by the ratio of gate and body capacitances, and  $V_{thfg-N}^0$  is the minimum observed  $V_{thfg-N}$ . Equation (1) is for N-FinFET, but may also be applied to a P-FinFET with usual changes in sign. If the FinFET is operated in SG mode, the threshold voltages of both gates respond simultaneously to change in voltage at the other gate. As shown in Equation (1), gate-gate coupling is observed only in the weak-inversion region of operation. In the region of strong inversion, the presence of inversion charge in the channel shields FinFET gate from each other and coupling becomes relatively weak.

As shown in Equation (1), the change of the back gate voltage can change the front gate threshold voltage, thus change the performance and leakage power. We want to use this feature in the 4T SRAM cell design to reduce the leakage and enhance the retention time. In order to test and quantify the back gate feature and its influence to leakage and performance, an inverter is tested. Due to the difficulty of measuring the threshold voltage, we use propagation delay time to show the performance. In Fig. 2, the back-gate voltages of N-FinFET and P-FinFET decrease and increase respectively. As a result, the front-gate threshold voltages of N-FinFET ( $V_{thfg-N}$ ) and P-FinFET ( $V_{thfg-P}$ ) increase and decrease respectively, which leads to an exponential decrease of leakage power, and the circuit propagation delay increases at the same time. But when the back-gate voltages exceed some boundaries ( $V_{thfg-N} = -0.3V$ ,  $V_{thfg-P} = 1.3V$ ), the threshold voltages of the front gate no longer follow the change of the back-gate voltages: The leakage power reduction and propagation delay in Fig. 2 match the theory (Equation 1) well. In the next part of paper, we are going to use this feature to reduce SRAM leakage power.

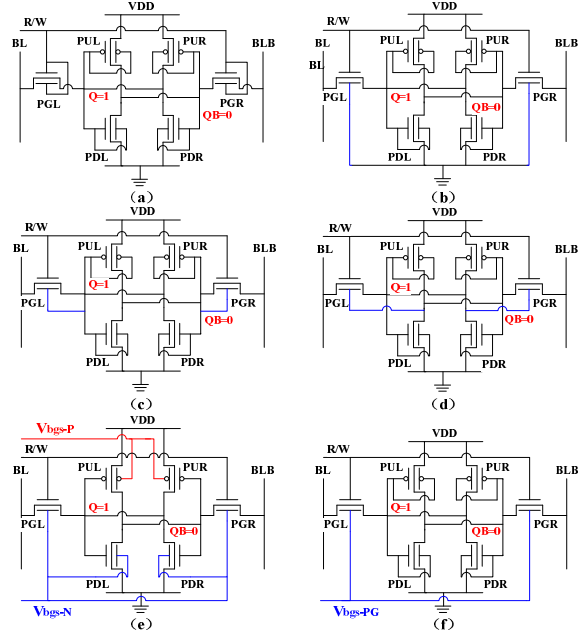


**Fig 2.** Back-gate bias voltage vs. power and delay. An LP-Mode inverter is tested. Input slew is 0.1ns. When the internal is tested, the output load is 0.0048726pF. When leakage is tested, output load is null.

### III. PREVIOUS WORK

Many FinFET SRAM cells have been proposed based on the FinFET back-gate characteristics. Fig. 3 (a) is the basic FinFET SRAM cell, deriving from traditional 6T CMOS SRAM cell. Fig. 3 (b) derives from the former one, the back-gate of whose PGL&PGR are connected to GND [13]. Fig. 3 (c) connects the back-gate to the twisted inverters to automatically change the threshold voltage of PGL&PGR [14]. While in Fig. 3(d), they are connected to the other nodes of the twisted inverters [15]. Fig. 3 (e) pulls all the nodes of

back-gate out, in this way, the threshold of all the FinFETs could be controlled [16]. While in Fig. 3 (f), only the back-gate voltages of PGL&PGR are controlled [16].

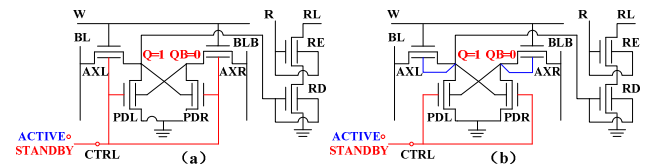


**Figure 3.** Previous FinFET SRAM cells [12-16]. Fin Height=40nm, L=32nm, Tox=1.4nm, Tsi=8.6nm. Pull-down FinFETs (PDL-PDR) uses 2 fins, others use 1 fin.

### IV. PROPOSED NOVEL 6T FINFET SRAM CELLS

#### A. Novel 6T FinFET SRAM Cells

The proposed new cells (Design (a) and Design (b)) are derived from 4T FinFET cells [15-18] (Fig. 4 (a, b)). In order to improve the performance, the read and write lines are separated. Further, the back gate voltage can be dynamically controlled. In Fig. 4 (a, b), it can switch between two static voltages: (1) STANDBY voltage to reduce the leakage; (2) ACTIVE voltage to improve the writing speed.



**Figure 4.** Proposed FinFET SRAM cells. Fin Height=40nm; L=32nm; Tox=1.4nm; Tsi=8.6nm; Pull-down FinFETs (PDL-PDR) uses 2 fins, others use 1 fin.

The following aspects are carefully considered in the proposed cell design:

a) Due to the elimination of the cross-coupled inverters, BL and BLB need to be set to VDD unless used for writing to overcome the retention time issue. For example, if BL and BLB = 0, Q=1, QB=0, because the data in Q is maintained by the capacitance, leakage path from AXL to BL or PDL to GND may degrade the node value.

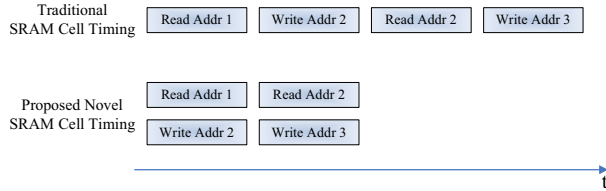
b) When the BL & BLB lines are used to write certain cells, the other cells in the same column need to keep Q and QB stable by parasitical capacitance, which causes a retention time issue as write disturb [18, 23]. Our design in Fig. 4 (a) use CTRL node connected to back-gate to mitigate such issue by reducing the leakage from Q and QB. For design in Fig. 4(b), the back-gates of AXL and AXR are connected to Q and QB, respectively, which increases the node capacitance of Q and QB.

c) The CTRL signal is determined by the ACTIVE and STANDBY modes, which is used to regulate back-gate voltage. At ACTIVE mode, the back-gate is connected to GND, while at STANDBY mode, the back-gate is  $-0.3$  V. The reason to avoid to apply much negative voltage than  $-0.3$  V is that, a more negative than  $-0.3$  V has trivial effect on the front gate threshold voltage, but it induces a large capacitance to increase the energy overhead during charge/discharge and causes an increase the leakage current at large range of back gate-voltage. The gate induced drain leakage may limit the technique of using control line to reduce leakage.

d) Half-select write disturb problem. The half select disturb occurs when there are certain unselected columns during a write operation while W is selected. In our design, the CTRL signal is used for a group of cells corresponding to the granularity of writing to mitigate this issue by adjusting the back-gate voltage of the pass-transistors in the unselected cells. This approach is a tradeoff between write margin and disturb margin. Other techniques can also be applied such as “read-then-write-back” scheme in [28].

e) The separation of read control signal (R) and read bit-line (RL) provides flexibility to adjust the read speed. RD & RE are connected to SG mode to enhance the read current and read speed. It also offers independent width design (fin numbers) of RD and RE without affecting the stability.

f) The separation of read and write lines allows read and write at the same cycle to different rows of cells. This feature may double the SRAM operating speed. As shown in Fig. 5, it takes 4 SRAM cycles to finish 4 operations in traditional SRAMs, while two cycles in for new cells.



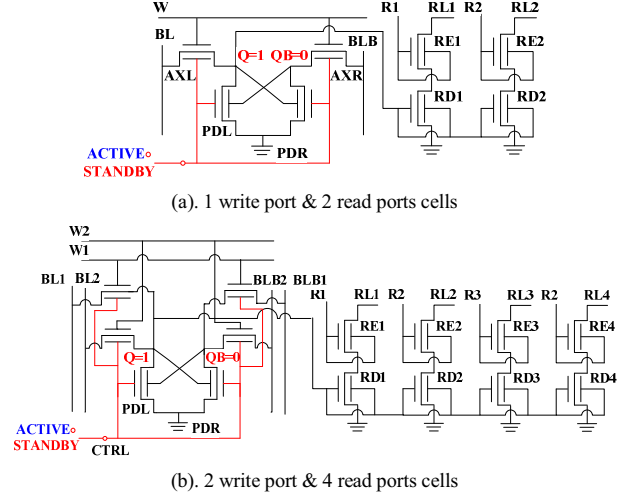
**Figure 5.** Comparison of timing between traditional and proposed FinFET SRAM cells.

g) Leakage reduction in Design (b). Compared to traditional 6T SRAM cells, the leakage current of PDL and PDR are different due to the back-gate control of AXL and AXR, which offers leakage reduction and data robustness. As shown in Fig. 4 (b), when  $Q=1$ , the connection to back-gate of AXL results a semi-conduction with enough current to maintain Q high. While AXR is closed at  $QB=0$ , the node QB is only supplied by the leakage of AXR, which is reduced by back-gate signal.

h) Both the new cells are made of N-FinFETs, which have no NBTI (Negative-bias temperature instability) reliability issue. NBTI is a result of continuous trap generation in the Si-SiO<sub>2</sub> interface of P-type transistors when the device is on [26, 27]. With the change of gate material, PBTI may also be a greater reliability issue than NBTI for HfO<sub>2</sub>/NiSi FETs: NBTI is observed to be independent of gate material whereas PBTI is significantly worse for FUSI gated devices [26]. PBTI in TiN and Re gated HfO<sub>2</sub> devices is much smaller than those observed for SiO<sub>2</sub>/HfO<sub>2</sub>/NiSi [26]. Thus, gate material for this kind of new cells needs to be carefully considered in fabrication.

### B. Multi-port Scalability of the Proposed Novel Cells

Multi-port SRAM is widely applied in register file designs. For example, when building the registers for the MIPS CPU, the single-issue structure needs 1 write port and 2 read ports for the register. For example, the R-type instructions, two registers’ data are used as inputs for ALU at the same time. For a VLIW (Very Long Instruction Word) technology, like 2-way, the register needs 2 write ports and 4 read ports. So the scalability of the SRAM cells is very important.



**Figure 6.** Multi-port scalability of the proposed novel cells.

Fig. 6 shows the possible scalability of the new-designed FinFET SRAM cells. The Fig. 6(a) shows a cell with 1 write port and 2 read ports. The modification is just to add another read port. This kind of modification is much easier than traditional 6T SRAM cells. Adding extra read ports actually makes the cell more stable, because the data in Q is maintained by capacitance; extra read ports actually make the capacitance larger. The shortcoming is that the write speed may be slower. The area overhead for an extra read port is 2 FinFETs, which is also smaller than the traditional ones.

Fig. 6(a, b) gives an example of a cell with 2 write ports and 4 read ports. The scalability of extra write ports requires extra AXL & AXR access FinFETs. As the number of write FinFETs connected to Q and QB increases, the leakage through the access FinFETs also increases, enhancing the stability of the cell. To further speed up the write speed, the write access FinFETs AXL&AXR can be connected in the SG mode. But the leakage will be larger, which is another trade-off offered by the proposed design.

## V. CHARACTERIZATION OF THE NEW CELLS

The following parameters are considered for performance evaluation: (1) leakage power dissipation and retention time, (2) stability during retention and read, (3) Write Margin, (4) Read and Write speed, (5) Area.

### A. Leakage and Retention Time

Leakage power takes the main part of the power, because most of the SRAM cells remain in standby for most time. There are two accesses to reduce leakage current: large  $L$  and high threshold voltage [20-22]. The former will lead to large area and the capacitance of word-lines & bit-lines, thus increases the read & write time and swells dynamic power. High threshold will result in low read current, negatively affecting read time. But this can improve the read & write margin. The new proposed cells dynamically adjust the threshold voltage [19-22]. In this way, the proposed cells overcome the shortcomings of high threshold voltage. As shown in Fig. 7, the leakage power reduces more than 80% compared to tradition 6T cells.

**Table I. Retention time of the proposed 6T cells**

Type	4T SG-FinFET Cell	6T SG-FinFET Cell*	Fig.4(a) BL,BLB=0	Fig.4(a) BL,BLB=1	Fig.4(b) BL,BLB=0	Fig.4(b) BL,BLB=1
Retention Time (ns)	5.7	6.3	55.6	169	2.7	$\infty$

\*The 6T SG-FinFET Cell is the cell similar to Fig.4 (a) and Fig.4(b), but AXL, AXR, PDL, PDR are connected with Short-gated Mode.

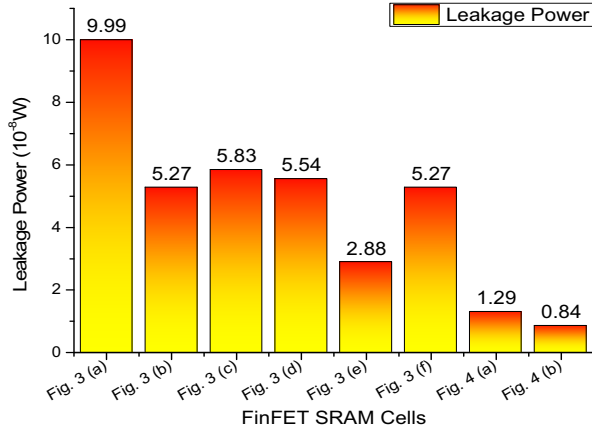


Figure 7. Leakage power comparison of FinFET SRAM cells.

Retention time is defined as the time from the last access to the time when the internal differential voltage of the cell ( $|Q-QB|$ ) drops below the detection threshold [18][32]. Table I shows the retention time comparison. The 4T SG-FinFET cell is derived from bulk-CMOS 4T cell, whose retention time is 5.7ns. The 6T SG-FinFET cell, whose structure is similar to Fig. 4(a, b), but AXL, AXR, PDL, PDR are in SG mode, shows a 6.3 ns retention time. This retention time is a little longer than 4T SG-FinFET cell, because the RD gate capacitance helped a little bit for the retention time. For Fig. 4(a) cell, when BL and BLB are low, the retention time is 55.6 ns; when BL and BLB are charged to VDD, the retention time is 169 ns, which is longer than 55.6 ns when BL, BLB=0, because when BL and BLB are charged to VDD, a small leakage current will flow from BL and BLB to Q and QB. While when BL, BLB=0, the leakage flows from Q=1 to BL or QB=1 to BLB. So the BL & BLB lines need to be charged to V<sub>DD</sub> to maintain the data in Q and QB. But when the cell in the same column is using BL & BLB to write data into the cell (either BL or BLB is 0), for the other cells in the same column, this situation is similar to “Fig. 4(a) BL, BLB=0” in Table I. So the retention time for Fig.4 (a) cell should be between 55.6 ns and 169 ns. For Fig. 4(b) cell, when BL and BLB are low, the retention time is only 2.7ns. The explanation is as follows. When Q is logical 1, the voltage of Q should be VDD-V<sub>th</sub> (Surely we can improve the word-line voltage to make it VDD), so the back-gate of AXL is VDD-V<sub>th</sub>, while BL is 0, the electric charge in Q will flow both through AXL to BL and PDL to ground. And this will also disturb the write operation to other cell. In the condition “Fig. 4(b) BL, BLB=1”, there are no retention time problem, because AXL is on (when Q=1), this will make the cell a stable one. In addition, the increase of capacitance in Fig. 4(b) cell (AXL’s back-gate capacitance to Q, AXR’s back-gate capacitance to QB) may also donate for the stability.

To solve the retention time problem for Fig. 4(a) cell, we need to re-fresh the cells during every retention time. As writing operation does not need a write pre-charge, we can just use buffers with strong driving ability to operate BL and BLB. For Fig. 4(b) cell, whose retention time is only 2.7 ns when BL and BLB are 0, we recommend a write pre-charge: to pre-charge BL and BLB during every writing operation. In the way, Fig 4(b) cell will be stable.

### B. Read, Write and Hold Static Noise Margin

In traditional 6T cells, during the read operation when Q=1, QB=0, QB increases. The amount of voltage increase at the node, denoted by  $V_{reads}$ , depends on the division of the (pre-charged) BLB voltage by the access transistor PGR and the pull-down transistor PDL. If  $V_{reads}$  is greater than the trip point of the right inverter (PUR-PDR), the cell changes its state causing a read failure. This read margin parameter can be computed by measuring the side of the largest square that can be fitted in the butterfly diagram [14-15, 24].

While in the proposed cells, the read signal affects Q through the gate of RD. Since the voltage division is caused by  $C_{gs}$ ,  $C_{gd}$  of RD is very much tinier compared to the division caused by direct current flow in the traditional cells, the read margin is very ideal as VDD-V<sub>th</sub> (Fig. 8). Due to different read structure, the read SNM is much better than that of the traditional ones.

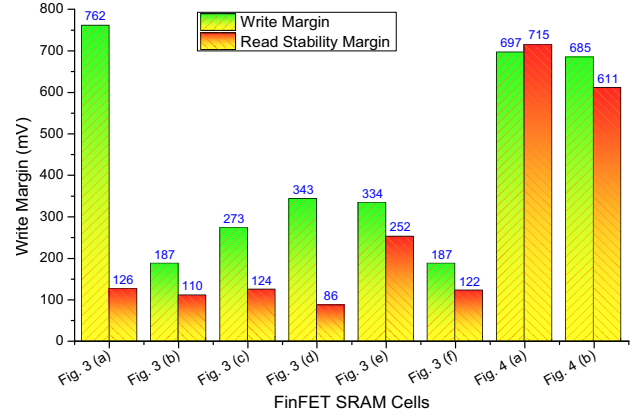


Figure 8. Write & Read comparison of FinFET SRAM cells.

During the write operation, the write margin is defined as the maximum decreased BL voltage that can change the state of the cell when BLB is kept high [14-15, 24]. The lower that value is, the harder it is to write the cell, implying a smaller write margin. The write margin characteristics for these cells are presented in Fig. 8, where the proposed cells are in high-level (697mV, 685mV). This is because the new cells use non-full-coupled inverters, the resistance to write into the cells is smaller than that of the traditional cells.

Due to the isolation feature (PGL & PGR are closed in hold time) of traditional cells in hold time and lack of PGL&PGR in proposed cells, the hold SNM is as the same as the read SNM.

### C. Read & Write Time

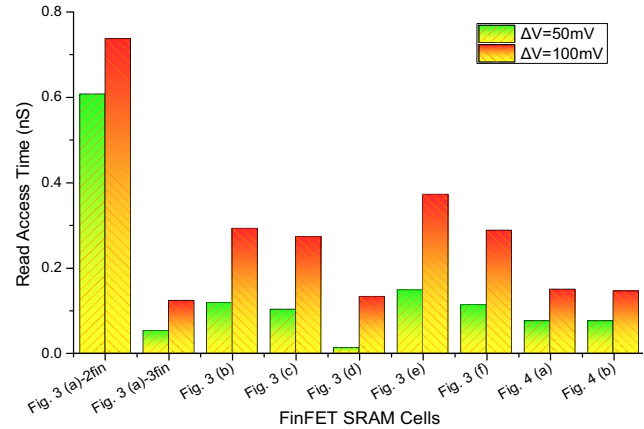


Figure 9. Read access time comparison.

Another important criterion in SRAM cell is the read time, which is the key factor of determining the SRAM speed. Because this factor also relates to the sensitive amplifiers’ sensitivity  $\Delta V$ , the amplifiers need to be carefully designed. Fig. 9 shows the comparison of read time feature. The Fig. 3(a)-2fin in means the Pull-down FinFETs in Fig. 3(a) has 2 fins (other FinFETs have 1 fin); Fig. 3(a)-3fin means Pull-down FinFETs have 3fins. The read speed of Fig. 3(a)-2fin is very slow because of the large write margin (as in Fig.8): during the read, the BL and BLB will disturb the cell with large glitch in Q and QB due to the large write margin. Compared to traditional cells, the



proposed two cells with separate read signal and read line have better performance in read time.

The write time, which is also an important SRAM parameter, is defined as the time that the word line is activated until the time that the storage node with '1' value decreases to the trip point of the inverter. The results are illustrated in Fig. 10, in which the proposed two cells have fast write time due to the weak coupling and small resistance to write in. While if we consider the parallelism of write & read to different addresses as in Fig. 5, the writing time is even faster.

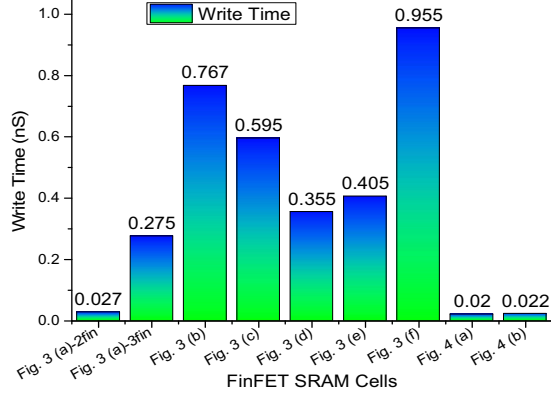


Figure 10. Write time comparison of FinFET SRAM cells.

#### D. Area

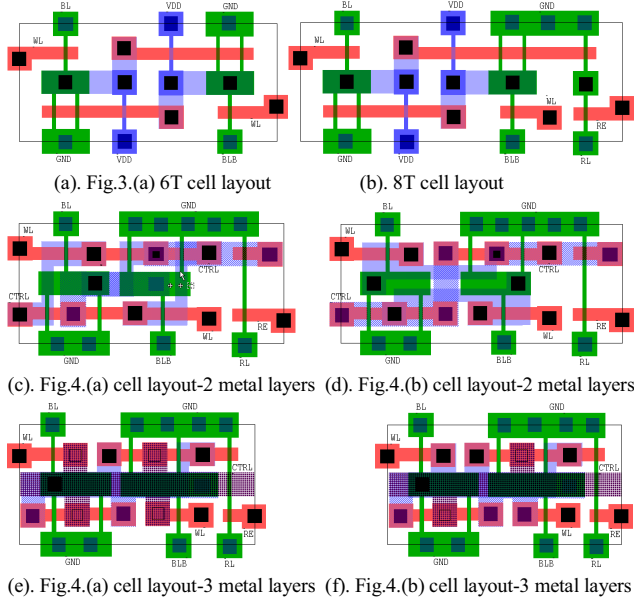


Figure 11. Thin-cell layout comparison. The Pull-down N-FinFETs have 2 fins, the Pull-up P-FinFETs : 1 fin, the access transistors AXL an AXR : 1 fin; the readout N-FinFETs : 1 fin.

Since physical design relates to performance, the parameters of each FinFET and layout should be carefully designed to satisfy the timing requirements and stability [24]. The RD/RE should be designed according to read time requirement. Fig. 11 shows an example of the possible thin cell layouts: Fig. 11 (a) is the layout of traditional 6T cells as Fig. 3 (a), Fig. 11(b) is the layout of 8T cell for comparison. The Fig. 11 (c, d) are layouts of the Fig. 4(a, b) cells with 2 metal layers: the word-line, RE and CTRL are in metal layer 1; BL, BLB, RL and GND are in metal layer 2. The Fig. 11 (e, f)

are layouts of the Fig. 4(a, b) cells with 3 metal layers: the CTRL signal is in metal layer 3.

The thin cell layout avoids bends in gate and orients all transistors in one direction, which is lithographically friendly and also reduces length and capacitance of bit-lines. Table II shows the summary of the thin cell layout area. The proposed Fig. 11(c) layout with 2 metal layers is as same area as the traditional 6T layout, but 11.4% smaller than the traditional 8T layout. The proposed Fig. 11(d) layout with 2 metal layers is 9.1% larger than the traditional 6T layout, but 11.4% smaller than the traditional 8T layout. But when building large scale SRAM, the proposed cells may be larger in area because they have 3 more global signals: R, RL, CTRL, although the proposed cells do not need VDD.

Table II. Comparison of the area of thin-cell layout

Layout	Fig.11 (a)	8T SG-FinFET Cell*	Fig.11 (c)	Fig.11 (d)	Fig.11 (e)	Fig.11 (f)
W*L(32n m*32nm)	22*10	27.5*10	22*10	24*10	19.5*10	19.5*10
Area>(*32 nm <sup>2</sup> )	220	275	220	240	195	195

\*8T Short-Gated FinFET is traditional 6T cell with separated read ports.

#### VI. 8K\*128 SCALE TESTING RESULT

We perform an analysis for a large scale memory using the proposed cells to evaluate their benefits and trade-offs.

One of the considerations is the interaction using the same BL & BLB lines. As mentioned in Section IV. A, that BL & BLB always remain VDD unless in writing to increase the retention time for proposed cells. When BL & BLB are used by other cells in the same column for write operation (example. SRAM cell row 1, col 1. In Fig. 12), the stored states of the cells in the same column using the same BL & BLB lines can be disturbed.

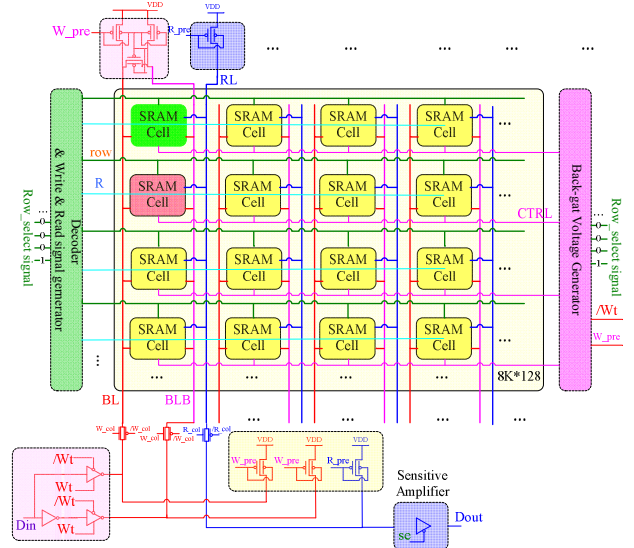


Figure 12. Structure and signals of 8K\*128 scale proposed cells.

To solve the potential write disturb issue, we ensure that the write time is several orders less than the retention time for our proposed designs. As shown in Table I, the minimum retention time is 55.6 ns and 2.7 ns for Design (a) and Design (b), respectively. Fig. 10 shows that the write time of the proposed cells is 20 ps and 22 ps for Design

(a) and (b), respectively, which satisfy the retention time requirement. Our results of the write time range are consistent of the previous 32nm FinFET designs in [31].

In Fig. 12, the CTRL signal (ACTIVE/STANDBY) is generated by special back gate voltage generator. Once the row signal is available and the operation is Write (this can be known by  $W_{pre}$  and  $Wt$ ), the back gate voltage generator changes the back gate voltage of that row from STANDBY (-0.3V) to ACTIVE (GND) to enhance the write speed. Fig. 13 shows the simulation results of proposed cell Fig. 4 (a). The voltages of Q and QB successfully maintain because of their parasitical capacitances and the dynamic adjustment of the back-gate voltage, whose main function is to increase the threshold and hence reduce the leakage current.

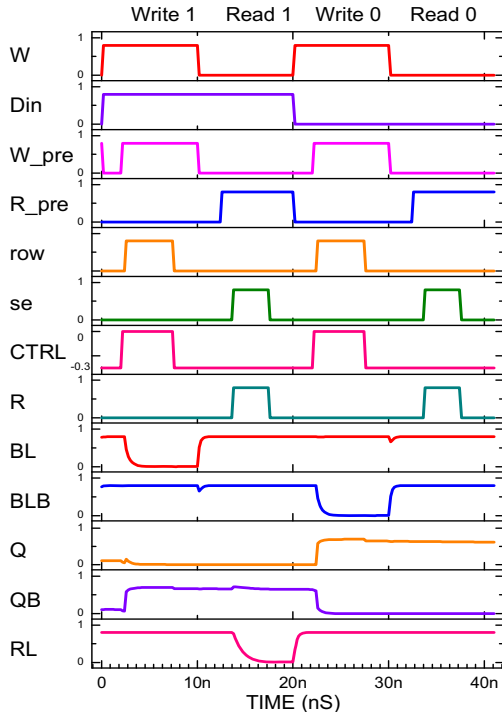


Figure 13. Simulation results of proposed cell as Fig. 4 (b).

## VII. CONCLUSION

The proposed 6T cells reduces more than 80% leakage current and bring great improvement in read margin, read and write speed. An 8K\*128 scale testing with all peripherals proves that the new two proposed FinFET SRAM cells can function well in large scale circuits. In addition, the newly proposed cells are easy for multi-port scalability. The new cells offer separate read and write timing and lines, which makes read & write to different cells at the same cycle possible, and this feature will greatly improve the access speed.

## REFERENCE

- [1] Niraj K. Jha, Deming Chen. "Nanoelectronic Circuit Design," 2011. Chapter: FinFET Circuit Design.
- [2] Gupta, S.K., et al, "Device-Circuit Co-Optimization for Robust Design of FinFET-Based SRAMs," IEEE Design & Test, vol.30, no.6, pp.29,39, Dec. 2013
- [3] Maszara, W.P. et al, "FinFETs - Technology and circuit design challenges," 2013 ESSCIRC, pp.3,8, 16-20 Sept. 2013
- [4] Sachid, A.B.; Chenming Hu, "Denser and More Stable SRAM Using FinFETs With Multiple Fin Heights," IEEE Transactions on Electron Devices, vol.59, no.8, pp.2037, 2041, Aug. 2012
- [5] Shien-Yang Wu, et al "A 16nm FinFET CMOS technology for mobile SoC and computing applications," IEDM, 2013

- [6] Min-Cheng Chen, et al. "A 10 nm Si-based bulk FinFETs 6T SRAM with multiple fin heights technology for 25% better static noise margin," 2013 VLSIT, pp.T218,T219, 11-13 June 2013
- [7] Sang Phill Park, et al. "Column-selection-enabled 8T SRAM array with  $\sim 1R/1W$  multi-port operation for DVFS-enabled processors," ISLPED 2011, vol., no., pp.303,308, 1-3 Aug. 2011
- [8] Gupta, S.K.; Kulkarni, J.P.; Roy, K., "Tri-Mode Independent Gate FinFET-Based SRAM With Pass-Gate Feedback: Technology-Circuit Co-Design for Enhanced Cell Stability," IEEE Transactions on Electron Devices, vol.60, no.11, pp.3696,3704, Nov. 2013
- [9] Jaksic, Z.; Canal, R., "Enhancing 6T SRAM cell stability by back gate biasing techniques for 10nm SOI FinFETs under process and environmental variations," 2012 MIXDES, pp.103,108, 2012
- [10] Hailong Jiao, et al. "Ground gated 8T SRAM cells with enhanced read and hold data stability," ISVLSI 2013, pp.52,57, 2013
- [11] Sarfraz, K, et al "Characterization of a low leakage current and high-speed 7T SRAM circuit with wide voltage margins," ISVLSI 2013,
- [12] Muttreja, A, et al. "Threshold Voltage Control through Multiple Supply Voltages for Power-Efficient FinFET Interconnects," VLSID 2008.
- [13] M. Yamaoka et al, "Low power SRAM menu for SOC application using Yin-Yang-feedback memory cell technology", in VLSI Circuits, 2004.
- [14] Zheng Guo, et al, "FinFET-based SRAM design," ISLPED '05. 2005.
- [15] Endo, K. et al. "Enhancing noise margins of FinFET SRAM by integrating  $V_{th}$ -controllable flexible-pass-gates," ESSDERC. 2008.
- [16] Giraud, B.; Amara, A.; Vladimirescu, A., "A Comparative Study of 6T and 4T SRAM Cells in Double-Gate CMOS with Statistical Variation," 2007. ISCAS 2007. , vol., no., pp.3022,3025, 27-30 May 2007
- [17] Endo, K. et al. "Independent-gate four-terminal FinFET SRAM for drastic leakage current reduction," ICICDT 2008. pp.63,66, 2-4 June 2008
- [18] Zhigang Hu, et al. "Managing leakage for transient data: decay and quasi-static 4T memory cells," ISLPED '02. pp.52,55, 2002
- [19] Endo, K. et al. "Enhancing SRAM cell performance by using independent double-gate FinFET," IEDM 2008.
- [20] Tawfik, S.A.; Zhiyu Liu; Kursun, V., "Independent-gate and tied-gate FinFET SRAM Circuits: Design guidelines for reduced area and enhanced stability," ICM 2007. pp.171,174, 29-31 Dec. 2007
- [21] Gupta, S.K.; Kulkarni, J.P.; Roy, K., "Tri-Mode Independent Gate FinFET-Based SRAM With Pass-Gate Feedback: Technology-Circuit Co-Design for Enhanced Cell Stability," IEEE Transactions on Electron Devices, vol.60, no.11, pp.3696,3704, Nov. 2013
- [22] Gupta, S.K.; Sang Phill Park; Roy, K., "Tri-Mode Independent-Gate FinFETs for Dynamic Voltage/Frequency Scalable 6T SRAMs," IEEE Trans. on Elec. Dev., vol.58, no.11, pp.3837, 3846, Nov. 2011
- [23] Zhiyu Liu; Tawfik, S.A.; Kursun, V., "Statistical Data Stability and Leakage Evaluation of FinFET SRAM Cells with Dynamic Threshold Voltage Tuning under Process Parameter Fluctuations," ISQED 2008. , vol., no., pp.305,310, 17-19 March 2008
- [24] Zhiyu Liu; Tawfik, S.A.; Kursun, V., "An independent-gate FinFET SRAM cell for high data stability and enhanced integration density," IEEE Int. SOC Conf., 2007, pp.63,66, 26-29 Sept. 2007
- [25] B. Ebrahimi and A. Afzali-Kusha, "NBTI tolerant 4T double-gate SRAM design", ULIS 2009. pp.221-224, 2009.
- [26] Zafar, S.; Kim, Y.-H.; Narayanan, V.; Cabral, C.; Paruchuri, V.; Doris, B.; Stathis, J.; Callegari, A.; Chudzik, M., "A Comparative Study of NBTI and PBTI (Charge Trapping) in SiO<sub>2</sub>/HfO<sub>2</sub> Stacks with FUSI, TiN, Re Gates," 2006 Symposium on VLSI Technology, 2006. Digest of Technical Papers. pp.23,25, 2006.
- [27] Yang, Hao-I; Ching-Te Chuang; Wei Hwang, "Impacts of NBTI and PBTI on power-gated SRAM with high-k metal-gate devices," ISCAS 2009. pp.377,380, 24-27 May 2009
- [28] Honda, K. et al. "Elimination of half select disturb in 8T-SRAM by local injected electron asymmetric pass gate transistor," CICC, 2010
- [29] Morita, Y., et al, "An Area-Conscious Low-Voltage-Oriented 8T-SRAM Design under DVS Environment," ISVLSI , 2007
- [30] Young Bok Kim; Yong-Bin Kim; Lombardi, Fabrizio, "New SRAM Cell Design for Low Power and High Reliability Using 32nm Independent Gate FinFET Technology," 2008 IEEE International Workshop on Design and Test of Nano Devices, Circuits and Systems, pp.25,28, 2008
- [31] NIMO Group at ASU, PTM: <http://ptm.asu.edu/>.
- [32] Sharma, V. et al. "Ultra Low-Energy SRAM Design for Smart Ubiquitous Sensors," Micro, 2012